

**VERIFICATION**

I, Yoshihiro KATO, of 2-11-12, Ebisu-Nishi, Shibuya-ku, Tokyo 150-0021 JAPAN, hereby declare that I am conversant with Japanese and English languages and that I am the translator of the documents attached and certify that to the best of my knowledge and belief the attached is a true and correct translation of:

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	[Name of Item]	Specification	1
5	[Name of Item]	Drawing	1
	[Name of Item]	Abstract	1

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[Title of the invention]

METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

[Claims]

- 5 1. A method of manufacturing a semiconductor device comprising:

forming an insulating film on a semiconductor substrate,
forming a concave in said insulating film and then forming a
metal film filling said concave;

- 10 conducting a first polishing over a whole surface of
said substrate to form a metal area filled in said concave;
and

- conducting a second polishing over said whole surface
of said substrate to remove parts of said metal area and of
15 said insulating film;

wherein said second polishing also removes a part of a
normal taper formed in an upper part of said metal area.

2. A method of manufacturing a semiconductor device comprising:

- 20 forming a first interconnection of a metal film on a
semiconductor substrate;

forming an insulating film such that it covers said
first interconnection;

- selectively removing said insulating film to form a via
25 hole reaching an upper surface of said first interconnection
and an interconnection trench connected to said via hole;

forming a metal film filling said via hole and said interconnection trench;

conducting a first polishing over a whole surface of said substrate to form a second interconnection filled in
5 said via hole and said interconnection trench as well as a connection plug; and

conducting a second polishing over said whole surface of said substrate to remove parts of said second interconnection and of said insulating film;

10 wherein said second polishing also removes at least a part of a normal taper formed in an upper part of said interconnection trench.

3. A method of manufacturing a semiconductor device comprising:

15 forming an insulating film on a semiconductor substrate;

forming a sacrificial film on said insulating film;

selectively removing said sacrificial film and said insulating film to form a concave in said insulating film and
20 then forming a metal film filling said concave;

conducting a first polishing over a whole surface of said substrate to form a metal area filled in said concave;
and

conducting a second polishing over said whole surface
25 of said substrate to remove parts of said metal area and of said insulating film;

wherein said second polishing also remove said sacrificial film.

4. The method as set forth in Claim 3, wherein said step of forming said concave in said insulating film comprises

5 conducting etching under an etching conditions in which said sacrificial film is more slowly etched than said insulating film.

5. A method of manufacturing a semiconductor device comprising:

10 forming a first interconnection of a metal film on a semiconductor substrate;

forming an insulating film such that it covers said first interconnection;

forming a sacrificial film on said insulating film;

15 selectively removing said insulating film and said sacrificial film to form a via hole reaching an upper surface of said first interconnection and an interconnection trench connected to said via hole;

forming a metal film filling said via hole and said
20 interconnection trench;

conducting a first polishing over a surface of said substrate to form a second interconnection and a connection plug filled in said via hole and said interconnection trench;
and

25 conducting a second polishing over said whole surface of said substrate to remove parts of said second

interconnection and of said insulating film;

wherein said second polishing also remove said sacrificial film on said insulating film.

6. The method as set forth in Claim 5, wherein said step of
5 forming said via hole and said interconnection trench in said insulating film comprises conducting etching under an etching conditions in which said sacrificial film is more slowly etched than said insulating film.

7. The method as set forth in any of Claim 1 through Claim 6,
10 wherein an information on a polishing rate in said second polishing is obtained and on a basis of said information, an end point of said second polishing is determined.

8. The method as set forth in any of Claim 1 through Claim 7,
wherein a thickness of said insulating film polished along
15 with said metal area is observed to determine an end point of said second polishing.

[Detailed description of the Invention]

[0001]

[Field to which the invention belongs]

This invention relates to a method of manufacturing a
5 semiconductor device. In particular, it relates to a method
of manufacturing a semiconductor device comprising damascene
interconnections.

[0002]

[Related art]

10 Recently, copper having a lower specific resistance has
been often used as a material for an interconnection in a
semiconductor device. Since it is difficult to perform
reactive ion etching on copper, the damascene process is
usually employed for forming the interconnection when using
15 copper as the interconnect material. Known damascene
processes include a single damascene process in which an
interconnection layer and a via hole are stepwise formed and
a dual damascene process in which an interconnection layer
and a via hole are simultaneously formed. Among these, a
20 dual damascene process is advantageous in the light of
reduction in the number of steps because the via hole and the
interconnection trench are simultaneously buried. The via
hole may be made of the same type of copper as that for the
interconnection to reduce a resistance of the via hole.

25 (Patent Document 1.)

[0003]

Forming an interconnection structure using a dual damascene process can be conducted by a via-first or trench-first process. In a via-first process, a via hole is first formed and an interconnection trench is then formed such that the trench is superposed over the via hole pattern. On the other hand, in a trench-first process, an interconnection trench is first formed and a via hole is then formed such that the via hole is superposed over the trench. The former is advantageous in the light of ensuring good contact performance of the via hole. Now referring to FIGS. 1 and 2 to 2D, conventional via-first steps of the dual damascene process will be described below.

[0004]

FIG 1A shows the step in which a first interconnection 103, diffusion barrier film 105 and a second insulating film 107 are sequentially formed on a substrate (not shown in the drawings). After depositing a first insulating film 101 on the substrate, an interconnection trench is formed by dry etching and then a barrier metal film (not shown in the drawings) and a copper film are formed in sequence such that the trench is filled with them. Then, extraneous barrier metal and copper films formed outside of the interconnection trench are removed by CMP (Chemical Mechanical Polishing), to form the first interconnection 103. Next, on the first interconnection 103 is formed the diffusion barrier film 105. The diffusion barrier film 105 is formed for preventing

copper from diffusing into the insulating film and is also used as an etching stopper film during forming a via hole 111. Then, on the diffusion barrier film 105 is formed the second insulating film 107.

5 [0005]

The second insulating film 107 is an interlayer insulating film having a lower dielectric constant. Thus, the structure of FIG. 1A is provided.

[0006]

10 Then, as shown in FIG. 1B, on the second insulating film 107 are sequentially formed an anti-reflection film (not shown in the drawings) and a resist film 109, and a resist pattern for the via hole 111 is formed by lithography. Then, the via hole 111 is formed by dry etching. During the
15 process, etching is stopped on the diffusion barrier film 105, utilizing a difference in an etching rate between the second insulating film 107 and the diffusion barrier film 105 for preventing copper contamination due to exposure of the first interconnection 103, ashing after etching and damage to the
20 copper during a washing procedure. After etching, the resist film 109 and the anti-reflection film are removed by ashing.

[0007]

Then, as shown in FIG. 1C, on the second insulating film 107 are sequentially formed an anti-reflection film (not
25 shown in the drawings) and a resist film 115, and then a resist pattern for the interconnection trench 117 is formed

as described above. Then, the interconnection trench 117 is formed by dry etching. During the process, the bottom of the via hole 111 is not etched because the anti-reflection film or the resist film 115 is buried.

5 [0008]

Then, as shown in FIG. 1D, the resist film 115 and the anti-reflection film are removed by ashing. Next, as shown in FIG. 2A, the diffusion barrier film 105 in the bottom of the via hole 111 is removed by dry etching to expose the
10 first interconnection 103.

[0009]

Then, as shown in FIG. 2B, a barrier metal film 119 and a copper film (not shown in the drawings) to be a seed layer for electroplating are sequentially formed by sputtering over
15 the whole surface of the second insulating film 107 including the via hole 111 and the interconnection trench 117.

Subsequently, a copper film 121 is buried in the via hole 111 and the interconnection trench 117 by electroplating.

[0010]

20 Then, as shown in FIGs. 2C and 2D, the extraneous copper film 121 and barrier metal film 119 are removed by CMP.

[0011]

As described above, there are formed the copper film 121, i. e., the second interconnection in the interconnection
25 trench 117, and the via hole connecting the first interconnection 103 with the second interconnection.

[0012]

[Patent document 1]

JP2002-203898A (entire text)

[0013]

5 [Problem to be solved]

However, we have found a new problem after
investigating the process shown in FIGs. 1 and 2.

Specifically, it has been found that during etching the
diffusion barrier film 105 in the bottom of the via hole 111
10 in the process shown in FIG. 2A, etching is relatively faster
in the corner of the second insulating film 107 in the upper
part of the interconnection trench 117 so that the film is
etched in the form of a normal taper as shown in FIG. 2.
Thus, in an interval between fine interconnections, a
15 distance in the upper part of the interconnection trench 117
is further reduced, causing a parasitic capacitance and also
short circuit failure.

[0014]

In view of the problems, an objective of this invention
20 is to provide a method of manufacturing a semiconductor
device in which a parasitic capacitance is inhibited between
metal films such as interconnections, plugs and pads.
Another object of this invention is to provide a method of
manufacturing a semiconductor device in which short circuit
25 is inhibited between metal films such as interconnections,
plugs and pads.

[0015]

[Means to solve the problem]

According to the present invention, there is provided a method of manufacturing a semiconductor device comprising:

5 forming an insulating film on a semiconductor substrate,
forming a concave in the insulating film and then forming a
metal film filling the concave; conducting a first polishing
over the whole surface of the substrate to form a metal area
filled in the concave; and conducting a second polishing over
10 the whole surface of the substrate to remove parts of the
metal area and of the insulating film; wherein the second
polishing also removes at least a part of the normal taper
formed in the upper part of the metal area.

[0016]

15 According to the manufacturing method of this invention,
the method comprises removing at least a part of the normal
taper formed in the upper part of the metal area so that a
parasitic capacitance or short circuit failure between metal
areas can be prevented in the normal taper.

20 [0017]

For example, for a semiconductor device comprising a
lower interconnection on the substrate, the normal taper
formed in the upper part of the concave before removing the
extraneous metal film is often formed during exposing the
25 lower interconnection.

[0018]

According to the present invention, there is provided a method of manufacturing a semiconductor device comprising:
forming a first interconnection of a metal film on a semiconductor substrate; forming an insulating film covering
5 the first interconnection; selectively removing the insulating film to form a via hole reaching the upper surface of the first interconnection and an interconnection trench connected to the via hole; forming a metal film filling the via hole and the interconnection trench; conducting a first
10 polishing over the whole surface of the substrate to form a second interconnection filled in the via hole and the interconnection trench as well as a connection plug; and conducting a second polishing over the whole surface of the substrate to remove parts of the second interconnection and
15 of the insulating film; wherein the second polishing also removes at least a part of a normal taper formed in the upper part of the second interconnection.

[0019]

The above method according to this invention comprises
20 removing at least a part of the normal taper formed in the upper part of the concave so that the taper formed in the upper part of the concave can be reliably and effectively prevented. A parasitic capacitance or short circuit failure between metal films filling the concave can be, therefore,
25 also reliably and effectively prevented in a dual damascene process.

[0020]

According to the present invention, there is provided a method of manufacturing a semiconductor device comprising:
forming an insulating film on a semiconductor substrate;
5 forming a sacrificial film on the insulating film; removing the sacrificial film and the insulating film in sequence to form a concave in the insulating film and then forming a metal film filling the concave; conducting a first polishing over the whole surface of the substrate to form a metal area
10 filled in the concave; and conducting the second polishing over the whole surface of the substrate to remove parts of the metal area and of the insulating film; wherein the second polishing also remove the sacrificial film.

[0021]

15 The above method according to this invention comprises forming the sacrificial film on the insulating film and then removing the sacrificial film so that the normal taper formed in the upper part of the concave can be reliably removed. A parasitic capacitance or short circuit failure between metal
20 films filling the concave can be, therefore, reliably and effectively prevented.

[0022]

In the methods of manufacturing a semiconductor device according to this invention, forming the concave in the
25 insulating film may comprise conducting etching under the etching conditions in which the sacrificial film is more

slowly etched than the insulating film. Etching under the above conditions can reduce a size of the taper formed in the upper part of the concave. Thus, it results in thinner polishing in the second polishing so that short circuit failure between interconnections can be much more effectively prevented.

[0023]

Etching conditions include, for example, the type of the insulating film, the type of an etching gas and a bias-voltage value. Specifically, when using an organic film as insulating film and a gas containing hydrogen and nitrogen as an etching gas, a material for a sacrificial film is preferably SiO_2 which is etching-resistant to the gas.

[0024]

According to the present invention, there is provided a method of manufacturing a semiconductor device comprising: forming a first interconnection of a metal film on a semiconductor substrate; forming an insulating film such that it covers the first interconnection; forming a sacrificial film on the insulating film; selectively removing the insulating film and the sacrificial film in sequence to form a via hole reaching an upper surface of the first interconnection and an interconnection trench connected to the via hole; forming a metal film filling the via hole and the interconnection trench; conducting a first polishing over a whole surface of the substrate to form a second

interconnection and a connection plug filled in the hole and the interconnection trench; and conducting a second polishing over the whole surface of the substrate to remove parts of the second interconnection and of the insulating film;

5 wherein the second polishing also remove the sacrificial film on the insulating film.

[0025]

In a dual damascene process, a parasitic capacitance or short circuit failure between metal films filling a concave
10 can be reliably and effectively prevented by forming the sacrificial film on the insulating film and removing it.

[0026]

In the method of manufacturing a semiconductor device according to this invention, removing at least a part of the
15 normal taper formed in the upper part of the concave may be conducted before removing parts of the metal area and of the insulating film. Thus, the normal taper formed in the upper part of the concave can be more reliably removed.

[0027]

20 In the method of manufacturing a semiconductor device according to this invention, forming the via hole and the interconnection trench in the insulating film may comprise conducting etching under the etching conditions in which the sacrificial film is more slowly etched than the insulating
25 film.

[0028]

Etching under the above conditions can reduce a size of the taper formed in the upper part of the interconnection trench. Thus, it results in thinner polishing in the second polishing so that short circuit failure between

5 interconnections can be much more effectively prevented.

[0029]

In the method of manufacturing a semiconductor device according to this invention, an information on a polishing rate in the second polishing may be obtained and on the basis
10 of the information, the end point of the second polishing may be determined.

[0030]

The manufacturing method according to this invention comprises obtaining information on a polishing rate in the
15 second polishing and conducting polishing for a period determined on the basis of the information, so that a polishing thickness can be controlled. Thus, the normal taper formed in the upper part of the concave can be more reliably removed.

20 [0031]

In the method of manufacturing a semiconductor device according to this invention, a thickness of the insulating film polished along with the metal area may be observed to determine the end point of the second polishing.

25 [0032]

The manufacturing method according to this invention

comprises conducting polishing while observing a thickness of the insulating film polished, so that a thickness of the insulating film polished can be controlled. Thus, the normal taper formed in the upper part of the concave can be further
5 reliably removed.

[0033]

[Embodiments of the invention]

In these embodiments, polishing is conducted such that a taper formed in the upper part of the metal area is removed,
10 to prevent a parasitic capacitance or short circuit failure between metal areas. Preferred embodiments will be described with reference to the drawings.

[0034]

(First Embodiment)

15 FIGS. 3 and 4 are process cross sections illustrating a process for manufacturing a semiconductor device according to this embodiment. FIG. 3A shows the step of forming a first insulating film 201, a first interconnection 203 in the first insulating film 201, a diffusion barrier film 205 and a
20 second insulating film 207 on a substrate (not shown in the drawings) in sequence.

[0035]

The structure in FIG. 3A is formed as described below. On a substrate is deposited a first insulating film 201 and
25 an interconnection trench is formed by dry etching. Then, barrier metal and copper films (not shown in the drawings)

are sequentially formed such that the inside of the trench is filled with them. Then, the extraneous barrier metal and the copper films formed outside of the interconnection trench is removed by CMP to form a first interconnection 203. Next, on
5 the first interconnection 203 is formed the diffusion barrier film 205. The diffusion barrier film 205 is formed for preventing copper as a material for the first interconnection 203 from diffusing into the insulating film and for being used as an etching stopper film during formation of a via
10 hole 211. On the diffusion barrier film 205 is formed a second insulating film 207. Thus, the structure in FIG. 3A is formed.

[0036]

The first interconnection 203 may be made of Al, W or
15 TiN in place of Cu. The diffusion barrier film 205 may be made of, for example, SiC or SiN. A thickness of the diffusion barrier film 205 is, for example, 25 nm to 100 nm both inclusive.

[0037]

20 The second insulating film 207 is made of, for example, SiOC having a specific dielectric constant of 3.5 or less. SiOC is sometimes represented as SiOCH and generally contains Si, O, C and H as constituent elements. The second insulating film 207 may be formed by an appropriate method
25 such as CVD. Other examples of a material which can be used include a variety of materials having a lower dielectric

constant; for example, hydrogenated siloxane (HSQ),
methyilsiloxane (MSQ), hydrogenated methyilsiloxane (MHSQ),
polyimide (PI), perfluorocarbon (PPFC), aromatic ether (PAE),
aromatic hydrocarbon (PAHC) and benzocyclobutene (BCB). A
5 film made of any of these materials can be formed by an
appropriate method such as CVD or spin coating. A thickness
of the second insulating film 207 is, for example, 500 nm to
2000 nm both inclusive.

[0038]

10 Next, as shown in FIG. 3B, on the second insulating
film 207 are sequentially formed an anti-reflection film (not
shown in the drawings) and a resist film 209, and then a
resist pattern for a via hole 211 is formed by lithography.
Then, a via hole 211 is formed by dry etching. During the
15 process, etching is stopped on the diffusion barrier film 205,
utilizing a difference in an etching rate between the second
insulating film 207 and the diffusion barrier film 205 for
preventing metal contamination due to exposure of the first
interconnection 203, ashing after etching, and damage to the
20 metal during a washing procedure. After etching, the resist
film 209 and the anti-reflection film are removed by ashing.

[0039]

Then, as shown in FIG. 3C, on the second insulating
film 207 are sequentially formed an anti-reflection film (not
25 shown in the drawings) and a resist film 215, and then a
resist pattern for the interconnection trench 217 is formed

as described above. Then, the interconnection trench 217 is formed by dry etching. During the process, the bottom of the via hole 211 is not etched because the anti-reflection film or the resist film 215 is buried.

5 [0040]

Then, as shown in FIG. 3D, the resist film 215 and the anti-reflection film are removed by ashing. Next, as shown in FIG. 4A, the diffusion barrier film 205 in the bottom of the via hole 211 is removed to expose the first

10 interconnection 203.

[0041]

In the process, as shown in FIG. 4A, an etching rate in the upper part of the interconnection trench 217 is higher so that the upper part of the interconnection trench 217 is

15 etched in a form of a normal taper.

[0042]

Then, as shown in FIG. 4B, a barrier metal film 219 and a copper film (not shown in the drawings) to be a seed layer for electroplating are sequentially formed by sputtering over the whole surface of the second insulating film 207 including the via hole 211 and the interconnection trench 217. The barrier metal film 219 may be made of, for example, high melting metals or high melting metal compounds such as Ta, TaN, TiN and TiSiN and a stack of these. A thickness of the barrier metal film 219 is, for example, 10 nm to 50 nm both inclusive.

[0043]

Subsequently, a copper film 221 is simultaneously buried in the via hole 211 and the interconnection trench 217 by electroplating. The copper film 221 may be made of the same material as that for the first interconnection 203. A thickness of the copper film 221 is, for example, 300 nm to 2000 nm both inclusive.

[0044]

Then, as shown in FIGs. 4C and 4D, the extraneous copper film 221 and barrier metal film 219 formed in the area except the concave are removed by CMP to provide a semiconductor device in which the copper film 221 in the interconnection trench 217 is the second interconnection. The CMP process is conducted in two steps, i. e., the first polishing where polishing is stopped on the surface of the barrier metal film 219 using a large polishing rate ratio between the copper film 221 and the barrier metal film 219 (FIG. 4C)) and the second polishing where the remaining barrier metal film 219 is polished (FIG. 4D). In this embodiment, the second polishing polishes and flattens, along with the barrier metal film 219, the second insulating film 207 and the copper film 221 in the taper formed in the upper part of the interconnection trench 217. Thus, a taper with a small interval between interconnections is removed so that even in a space between fine interconnections, short circuit failure can be effectively prevented.

[0045]

In the first polishing, a slurry is used, whereby the copper film 221 is efficiently polished. Such a slurry may contain, for example, an oxidizing agent such as H_2O_2 and a corrosion inhibitor for a constituent metal in the copper film 221.

[0046]

In the second polishing, a slurry mainly for mechanical polishing is used for efficient polishing of the barrier metal film 219. Such a slurry may contain, for example, abrasive grains such as silica and a corrosion inhibitor for a constituent in the copper film 221. Since the second insulating film 207 and the copper film 221 are polished along with the barrier metal film 219, a slurry with which a difference in a polishing rate between these films is small is used. It is preferable to use a slurry in which, for example, a polishing rate ratio of the insulating film to the barrier metal is 1/3 to 3 both inclusive. Thus, dishing or erosion can be prevented and the polished surface can be kept flat.

[0047]

In the second polishing, all tapers in the upper part of the interconnection trench 217 may be polished or some of the tapers may be polished as long as short circuit failure does not occur. Since a taper formed in the upper part of the interconnection trench 117 is often formed to a depth of

about 50 nm or more when using a film having a lower dielectric constant such as SiOC as the second insulating film 207, it is particularly effective to polish the second insulating film 207 to 50 nm or more from the upper surface in the second polishing for preventing a parasitic capacitance or short circuit failure.

[0048]

Thus, in the manufacturing process of this embodiment, a polishing thickness needs to be controlled for efficiently removing a taper in the second polishing. A controlling method will be described.

[0049]

One of methods for controlling a polishing thickness is measurement of an interval between the upper surfaces of the interconnection trenches 217. The method will be described with reference to FIG. 7. FIG. 7 is an enlarged view of the upper part of the interconnection trench 217 in FIG. 2C.

[0050]

On a dummy wafer is formed an interconnection pattern in FIG. 4C as shown in FIGs. 3 and 4. Then, varying a polishing time in the second polishing (the arrows in FIG. 7), the upper surface of interconnection trench 217 in each stage is observed by, for example, SEM (scanning electron microscopy). CD-SEM is preferable because of more precise observation. The polishing conditions can be set such that an interval width between the interconnection trenches 217 is

measured and polishing is stopped when the width reaches a given value, to conveniently and efficiently control the thickness of the second insulating film 207 polished in the second polishing.

5 [0051]

In setting the polishing conditions, an actual wafer may be used instead of a dummy wafer.

[0052]

Alternatively, a polishing thickness can be controlled
10 by a method where a light interference type of thickness meter placed in a CMP apparatus is used as a module for detecting an end point as shown in FIG. 8. For example, a CMP apparatus, ISRM (in Situ Removal Monitor, from Applied Materials Inc.) may be used. In FIG. 8, in polishing pad 131
15 is formed a transparent window 133, into which a light enters. When a wafer 135 is above over the transparent window 133, a light entering the transparent window 133 is reflected and from interference thus generated, a thickness of the insulating film in the surface of the wafer 135 can be
20 determined. Employing such a configuration allows determination of a thickness when a barrier metal becomes absent in each wafer 135 during CMP. Thus, a thickness of the second insulating film 207 to be polished can be controlled by determining reduction in a thickness and then
25 stopping polishing when the thickness is reduced to a given level.

[0053]

(Second Embodiment)

FIGs. 5 and 6 show a process for manufacturing a semiconductor device according to this embodiment. The procedure to the configuration in FIG. 5A is as described in First Embodiment. FIG. 5A shows that a sacrificial film 213 is formed on the upper surface of the second insulating film 207 in FIG. 3A.

[0054]

10 The procedure in FIG. 5B and later is conducted as described in the procedure in FIG. 3B and later in First Embodiment to form a via hole 211 and an interconnection trench 217, then, on a sacrificial film 213 including the interconnection trench 217 and the second insulating film 207, 15 a barrier metal film 219 and a copper film 221 are formed. Thus, the cross section in FIG. 6B is provided.

[0055]

Subsequently, as shown in FIGs. 6C and 6D, two-step CMP is conducted as described in First Embodiment. In the second 20 polishing, the barrier metal film 219 and the tapered sacrificial film 213, the copper film 221 are polished to remove the sacrificial film 213. A polishing level in the second polishing is controlled, for example, as described in First Embodiment. Thus, the semiconductor device in FIG. 6D 25 in which the copper film 221 in the interconnection trench 217 is the second interconnection.

[0056]

A material for the sacrificial film 213 may be selected from those exhibiting an etching rate equal to or lower than that of the diffusion barrier film 205. A film exhibiting an etching rate lower than that of the diffusion barrier film 205 gives an etching rate lower than that of the second insulating film 207, so that formation of a taper in the upper part of the interconnection trench 217 can be prevented. For example, when using SiC as a material for the diffusion barrier film 205, a film exhibiting an etching rate equal to or lower than that of SiC, such as SiO₂, SiN, SiC, SiON and SiCN, can be used. A thickness of the sacrificial film 213 is, for example, 10 nm to 100 nm both inclusive. The film with a thickness of 10 nm or more can suitably prevent taper formation in the upper part of the interconnection trench 217 and thus can reduce a taper size. Furthermore, the film with a thickness of 100 nm or less can be efficiently removed in CMP.

[0057]

Thus, in this embodiment, the sacrificial film 213 exhibiting an etching rate lower than that of the second insulating film 207 is formed on the second insulating film 207, so that etching of the corner can be prevented in the upper part of the interconnection trench 217. A taper size formed in the upper part of the interconnection trench 217 can be reduced in comparison with the case where a

sacrificial film 213 is not formed. Therefore, as shown in FIG. 9, a polishing level in the second polishing can be reduced in comparison with the case in FIG. 7, for example, 30 nm. FIG. 9 is an enlarged view of the upper part of the interconnection trench 217 in FIG. 6C.

[0058]

Thus, in this embodiment, the sacrificial film 213 is formed on the second insulating film 207, to more efficiently remove the taper in the upper part of the interconnection trench 217. Short circuit between interconnections can be, therefore, more effectively prevented. Furthermore, since the sacrificial film 213 is removed by CMP, it is not necessary to take detachment from the second insulating film 207 into account. Thus, we can focus on performance as a sacrificial film 213, resulting in higher freedom in material selection.

[0059]

Although the present invention has been described by way of exemplary embodiments, it should be understood that many changes and substitutions may be made by those skilled in the art without departing from the spirit and the scope of the present invention which is defined only by the appended claims.

[0060]

[Effects of the invention]

As described above, according to the present invention,

there is provided a method of manufacturing a semiconductor device comprising: conducting a first polishing over the whole surface of the substrate to form a metal area filled in the concave; and conducting a second polishing over the whole surface of the substrate to remove parts of the metal area and of the insulating film, wherein the second polishing also removes at least a part of the normal taper formed in the upper part of the metal area and then a parasitic capacitance is inhibited between metal films such as interconnections, plugs and pads. In further accordance with the present invention, there is provided a method of manufacturing a semiconductor device in which short circuit is inhibited between metal films such as interconnections, plugs and pads.

[Brief description of the drawings]

FIG. 1 is a process cross section illustrating a process for manufacturing a semiconductor device of the related art.

FIG. 2 is a process cross section illustrating a process for manufacturing a semiconductor device of the related art.

FIG. 3 is a process cross section illustrating a process for manufacturing a semiconductor device according to an embodiment of this invention.

FIG. 4 is a process cross section illustrating a process for manufacturing a semiconductor device according to an embodiment of this invention.

FIG. 5 is a process cross section illustrating a process for manufacturing a semiconductor device according to an embodiment of this invention.

FIG. 6 is a process cross section illustrating a process for manufacturing a semiconductor device according to an embodiment of this invention.

FIG. 7 illustrates a method for controlling a polishing thickness according to an embodiment of this invention.

FIG. 8 illustrates a method for controlling a polishing thickness according to an embodiment of this invention.

FIG. 9 illustrates a method for controlling a polishing thickness according to an embodiment of this invention.

[Description of reference symbols]

101	first insulating film
103	first interconnection
105	diffusion barrier film
107	second insulating film
109	resist film
111	via hole
115	resist film
117	interconnection trench
119	barrier metal film
121	copper film
131	polishing pad
133	transparent window
135	wafer

- 201 first insulating film
- 203 first interconnection
- 205 diffusion barrier film
- 207 second insulating film
- 5 209 resist film
- 211 via hole
- 213 sacrificial film
- 215 resist film
- 217 interconnection trench
- 10 219 barrier metal film
- 221 copper film

[Name of Document] ABSTRACT OF THE DISCLOSURE

[Abstract]

[Problems]

To provide a method of manufacturing a semiconductor
5 device in which a parasitic capacitance is inhibited between
metal films and to provide a method of manufacturing a
semiconductor device in which short circuit is inhibited
between metal films.

[Means for solving the Problems]

10 On a substrate are sequentially formed a first
interconnection 203, a diffusion barrier film 205 and a
second insulating film 207, and on the upper surface of the
second insulating film 207 is then formed a sacrificial film
213. Next, a via hole 211 and an interconnection trench 217
15 are formed, and on the sacrificial film 213 are then formed a
barrier metal film 219 and a copper film 221. CMP for
removing the extraneous copper film 221 and barrier metal
film 219 are conducted in a two-step process, i. e., the
first polishing where polishing is stopped on the surface of
20 the barrier metal film 219 and the second polishing where the
remaining barrier metal film 219 and the tapered sacrificial
film 213 are polished.

[Selected Figure] Figure 4

1/8

FIG.1A

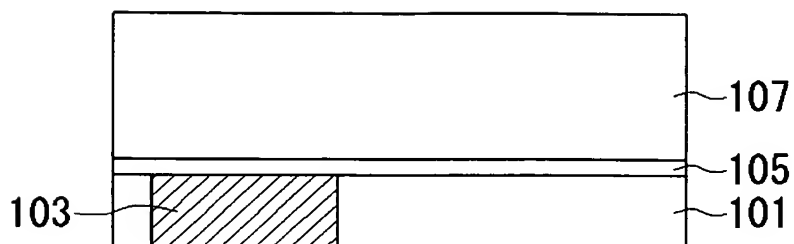


FIG.1B

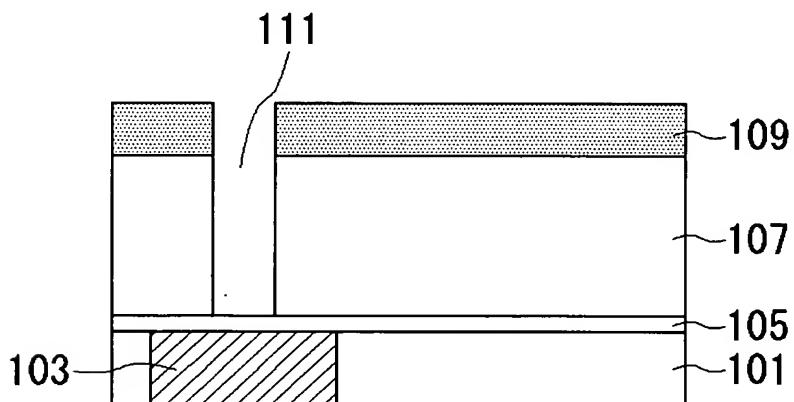


FIG.1C

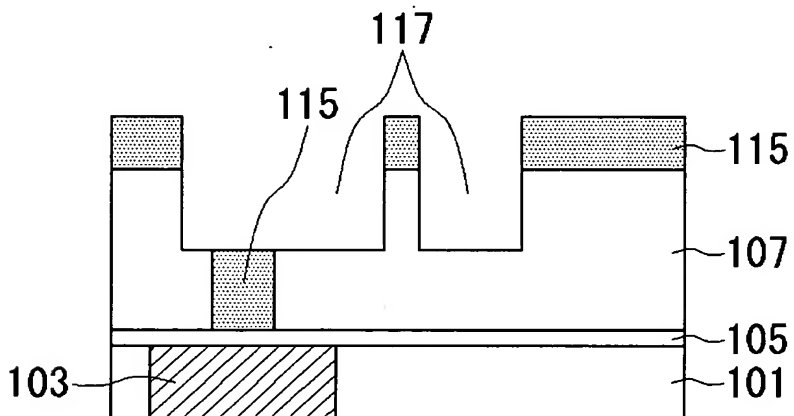


FIG.1D

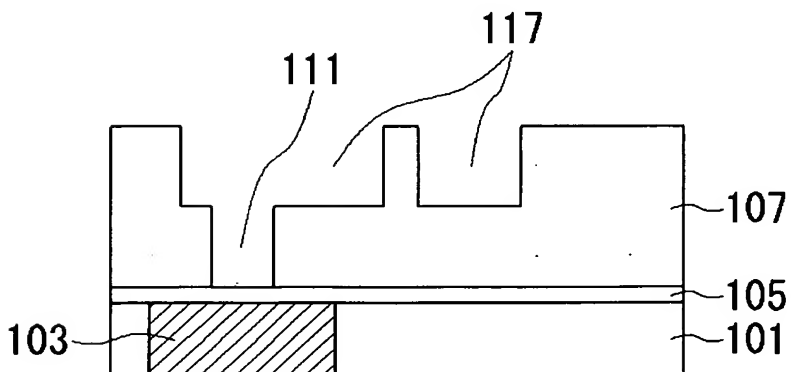


FIG.2A

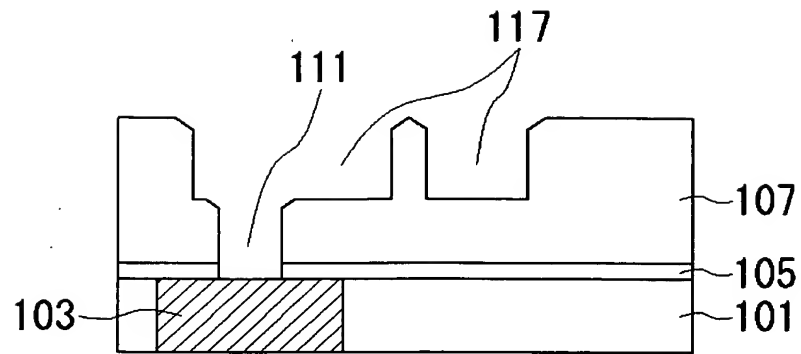


FIG.2B

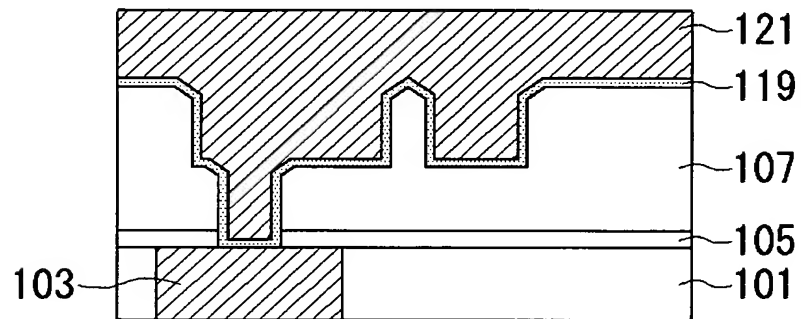


FIG.2C

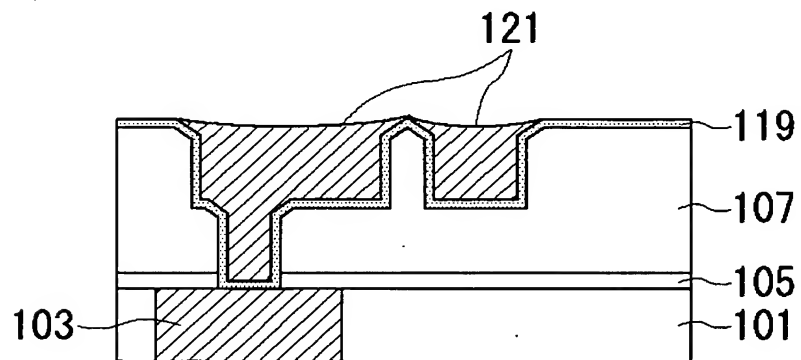


FIG.2D

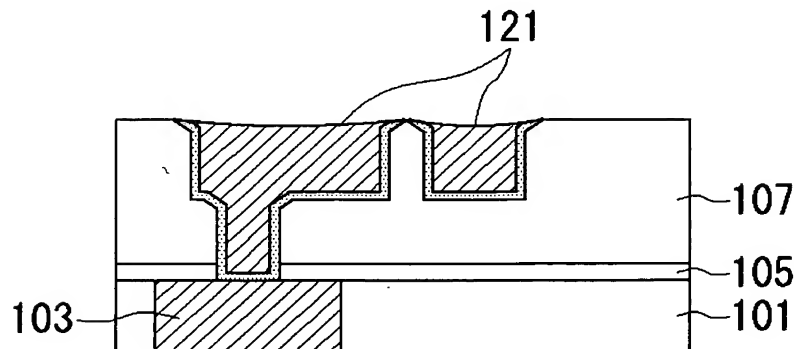


FIG.3A

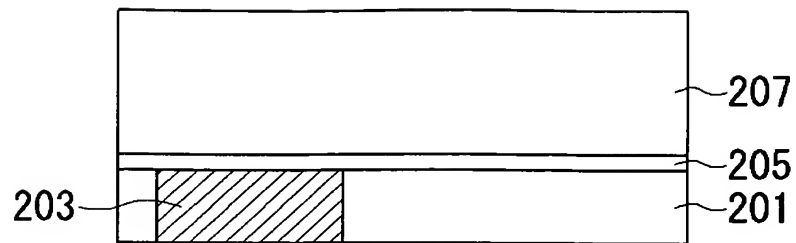


FIG.3B

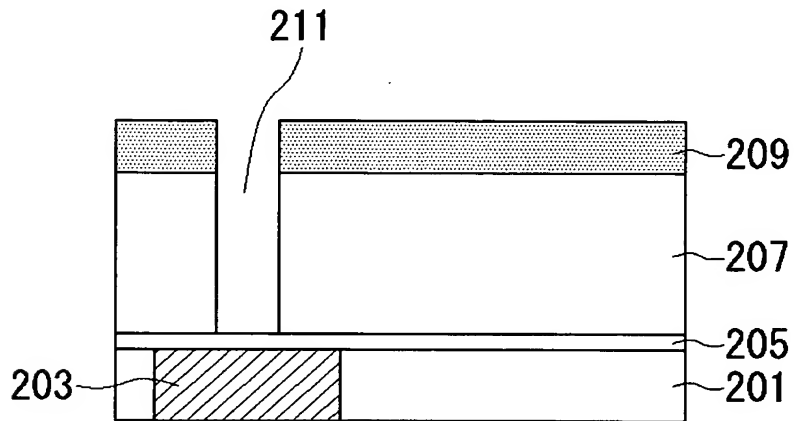


FIG.3C

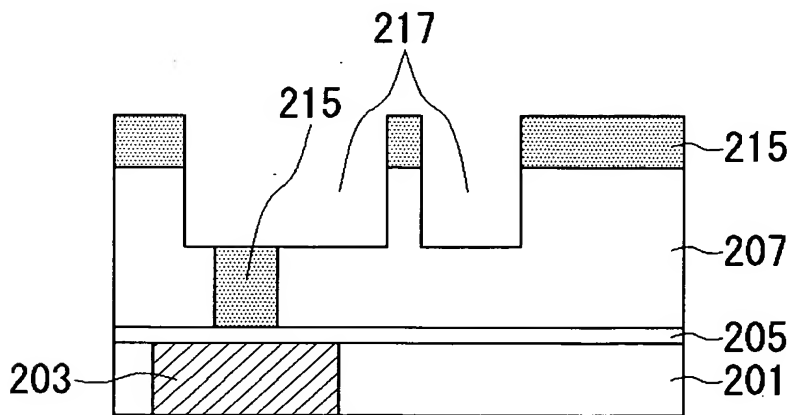


FIG.3D

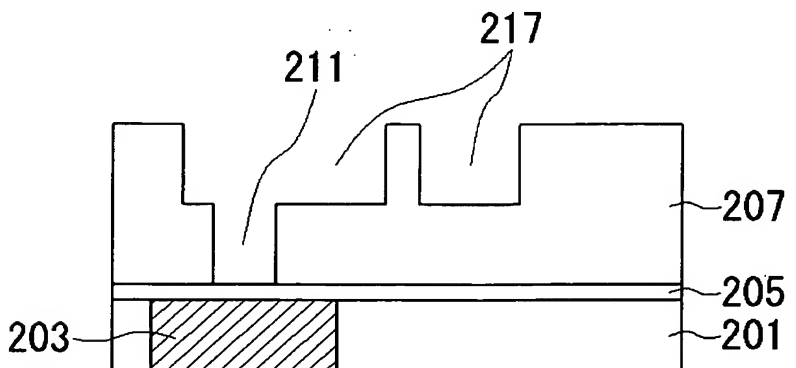


FIG.4A

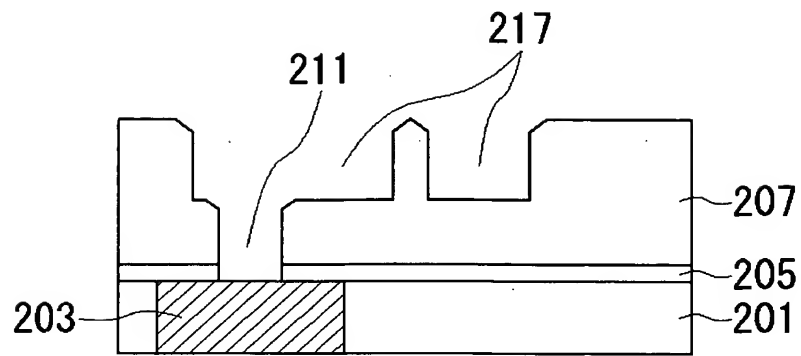


FIG.4B

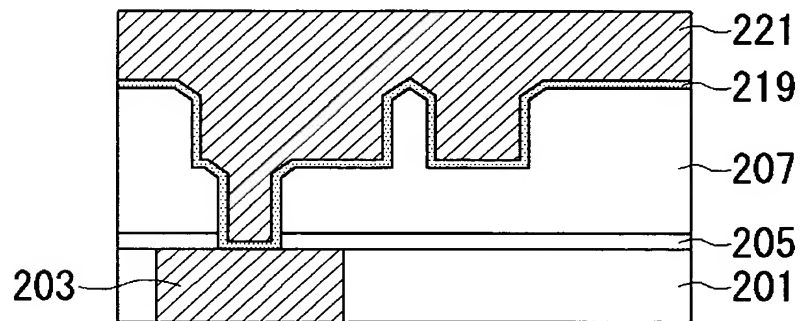


FIG.4C

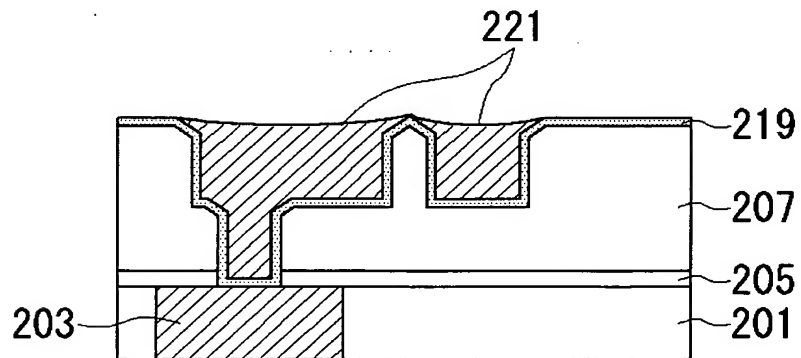


FIG.4D

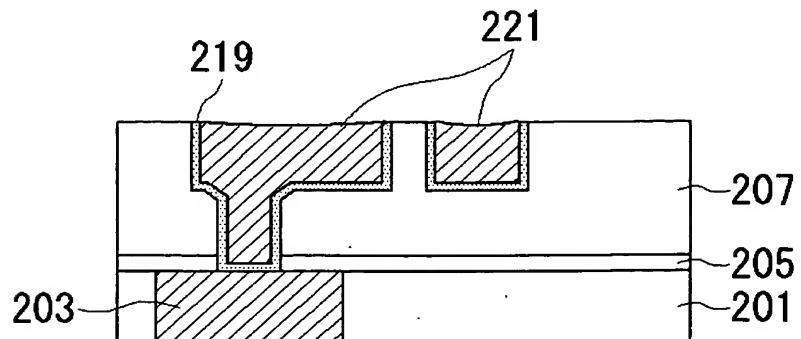


FIG.5A

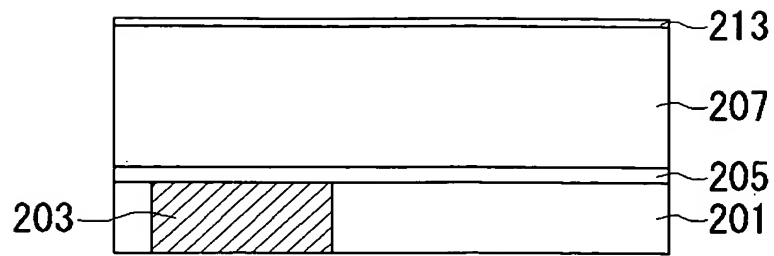


FIG.5B

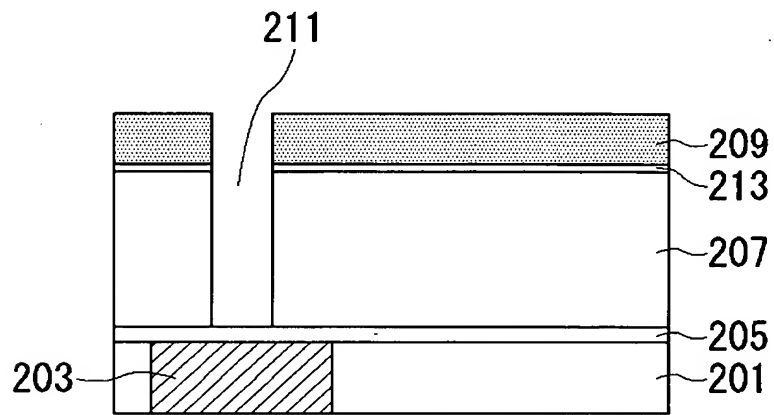


FIG.5C

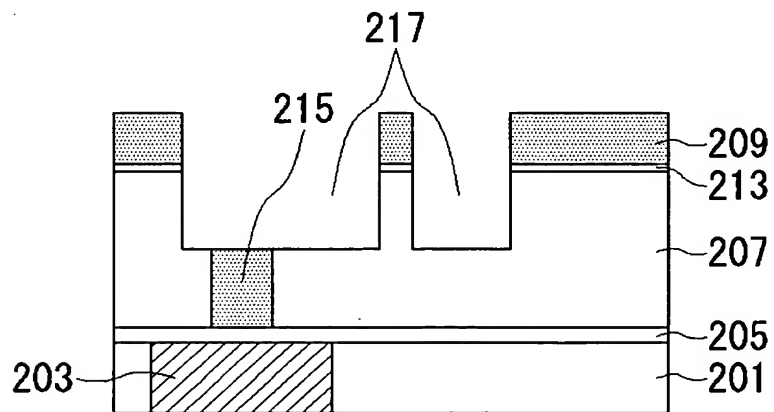


FIG.5D

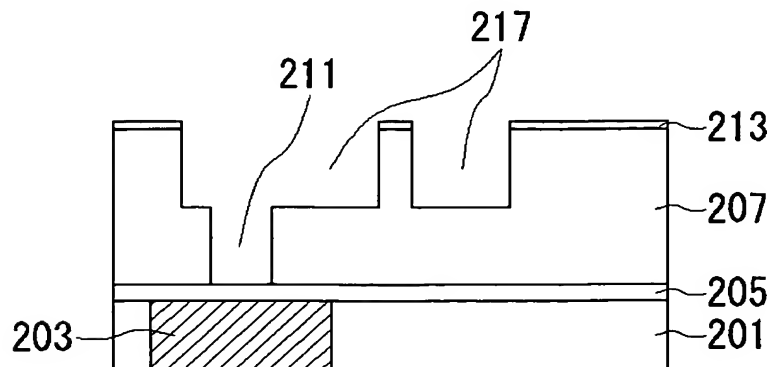


FIG.6A

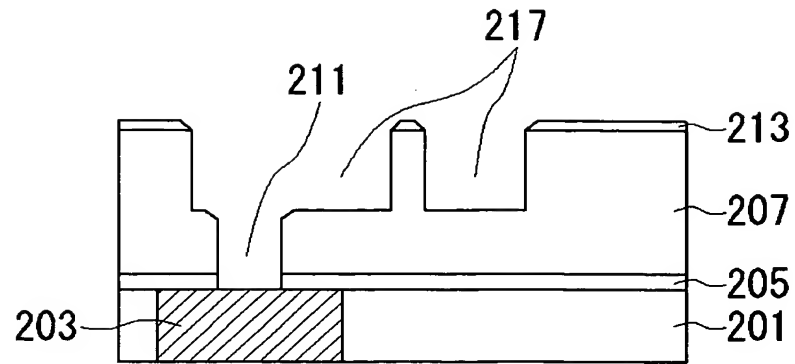


FIG.6B

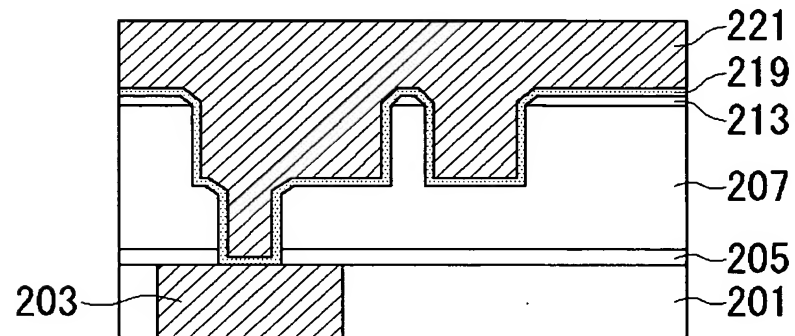


FIG.6C

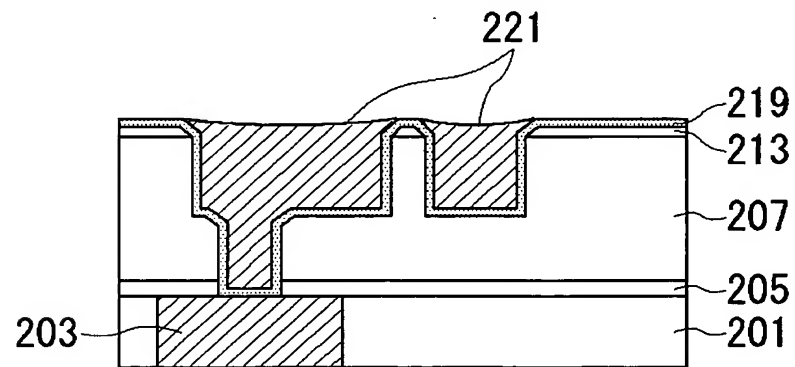


FIG.6D

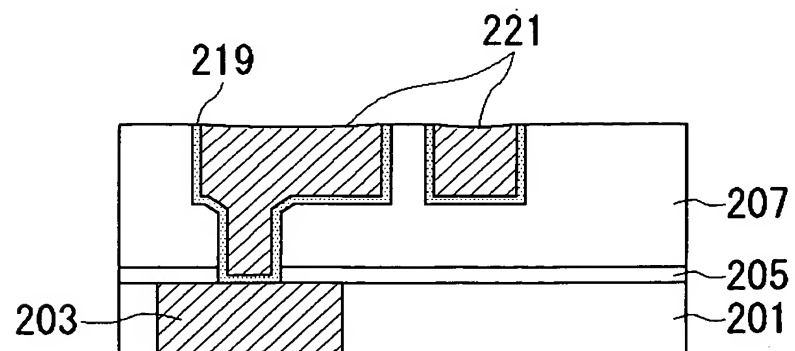


FIG.7

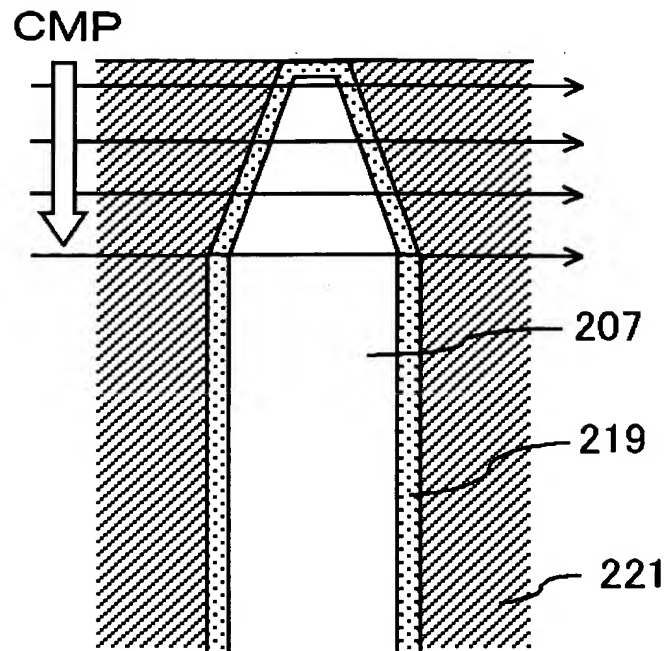


FIG.8

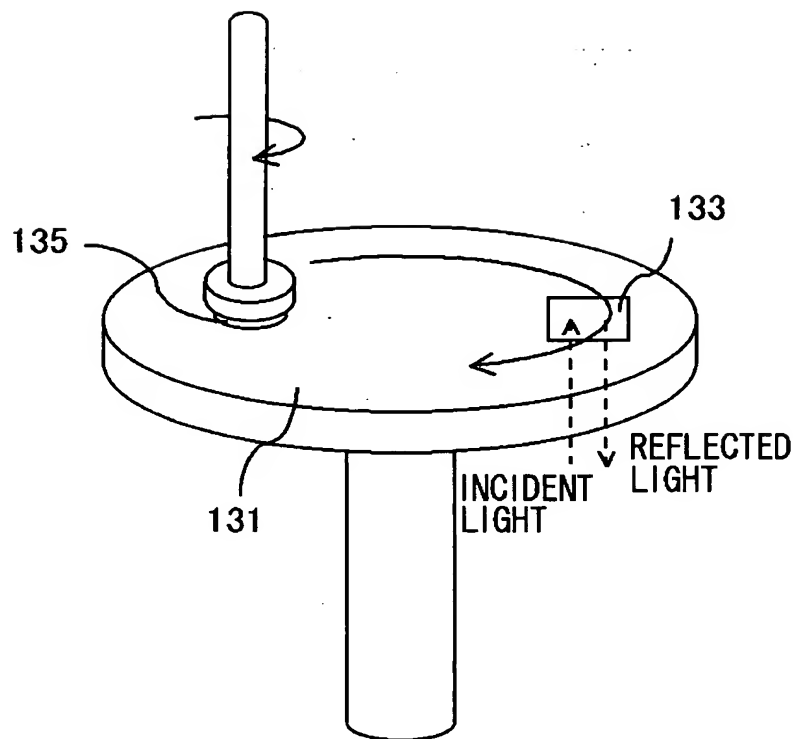


FIG.9

